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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,601	08/28/2003	Shi-Chi Lin	TS01-999	8321

54657 7590 10/04/2005

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,601	LIN, SHI-CHI	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *21 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☒ Claim(s) *12-18* is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 3 recites the formation of a silicon dioxide liner. The recited limitation of a silicon dioxide liner is confusing and should be corrected so that it makes clear that this liner is the same dielectric layer or silicon dioxide as previously recited in claim 2.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 6, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. No. 5,110,755) in view of Lin et al. (US Pat. No. 6,436,791 B1).

Regarding claim 1, Chen et al. teaches a method of providing an intermediate dielectric isolated silicon structure comprising the steps of:

forming a trench pattern (15) on a semiconductor substrate (1) (see fig. 1B);

forming a heavily doped buried p^+ layer (19) around said trench pattern (15) (see fig. 1C);

depositing silicon (23) to said trench pattern (see fig. 1D);

forming buried porous silicon layer (25) around said filled trench pattern (see fig. 1E);

oxidizing said buried porous silicon layer (27) and forming a thin oxide (29) over said deposited silicon surface (see fig. 1F); and

forming isolated silicon islands (23) from said deposited silicon (see fig. 1F).

However, Chen et al. fails to teach the steps of forming a dielectric layer on the surfaces of said trench pattern; and exposing semiconductor surface on the bottom of said trench pattern.

Lin et al. teaches that it is well known in the art to form an oxide layer (130) in a trench (125) and to remove the oxide (130) to expose the bottom surface (102) of the trench (130) and to form spacers (132) (see figs. 3-4).

Lin et al. and Chen et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include the steps of forming a dielectric layer on surfaces of a trench pattern; and exposing a semiconductor surface on the bottom of said trench pattern. The motivation for doing so is to reduce defects by inhibiting deposition of epitaxial silicon on sidewalls of the trench and to facilitate the subsequent filling of the trench. Therefore, it would have been obvious to combine Lin et al. with Chen et al. to obtain the invention of claims 1-3, 6, 9 and 11.

Regarding claim 2, Lin et al. teaches that the dielectric layer (130) is a silicon oxide layer deposited by CVD (see col. 2, lines 41-44).

Regarding claim 3, Lin et al. teaches that the silicon oxide layer (130) is approximately 2000 Å (see col. 2, lines 45-46).

Regarding claim 6, Chen et al. teaches a selective epitaxial silicon (23) (see col. 5, lines 15-16).

Regarding claim 9, Chen et al. teaches that said porous silicon layer is oxidized at about 1000 °C (see col. 5, lines 53-54).

Regarding claim 11, Lin et al. teaches removing the thermal oxide (150) on the epitaxial silicon layer (140) (see figs. 4-5) by etching or CMP (see col. 3. lines 4-8).

6. Claims 4-5, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. No. 5,130,268) in view of Lin et al. (US Pat. No. 6,436,791 B1), and further in view of Lin et al. (US Pat. No. 5,950,094).

Regarding claims 4-5, 8 and 10, a further difference between the prior art and the claimed invention is dose of the boron implantation, the thickness of the implanted region and the etching bath composition and current density of the anodic etching process.

Lin et al. ('094) teaches that it is well known in the art to form a porous layer by implanting boron ions at a dose of between 10^{15} and 10^{16} atom/cm^2 and anodizing the implanted region having a thickness of 4000 Å by using an etching bath composition of 10%-40% HF and a current density of 10-60 mA/cm^2 (see col. 3, lines 15-20, 24-26 and

45-49). Further, Lin et al. teaches the step of completely oxidizing the implanted region, which inherently results in an oxide region having about the same thickness (i.e. 4000 Å) as the implanted region prior being oxidized (see col. 3, lines 60-62).

Lin et al., Lin et al. ('094) and Chen et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further form a porous layer by implanting boron ions at a dose of between 10^{15} and 10^{16} atom/cm^2 and anodizing the implanted region having a thickness of 4000 Å by using an etching bath composition of 10%-40% HF and a current density of 10-60 mA/cm^2, and oxidizing the anodized implanted region layer to form an oxide layer having thickness of about 4000 Å. The motivation for further doing so, as is taught by Lin et al. ('094), is allowing a thicker and wider isolation region (col. 3, lines 39-44). Therefore, it would have been obvious to further combine Lin et al. ('094) with Lin et al. and Chen et al. to obtain the invention of claims 4-5, 8 and 10.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. No. 5,130,268) in view of Lin et al. (US Pat. No. 6,436,791 B1), and further in view of Wolf (Silicon Processing for the VLSI Era, Vol. 1-Process Technology, 156-157).

Regarding claim 7, a further different is the technique used to epitaxially growing the silicon layer. Wolf teaches that it is well known in the art to form an epitaxial silicon layer by MBE (see page 156-157).

Wolf, Lin et al. and Chen et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further form an epitaxial silicon layer by MBE. The motivation for further doing so, as is taught by Wolf, is growing a layer at low temperatures, which reduce outdiffusion and autodoping effects (page 156-157). Therefore, it would have been obvious to further combine Wolf with Lin et al. and Chen et al. to obtain the invention of claim 7.

Allowable Subject Matter

8. Claims 12-18 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a method comprising the step of forming a resist pattern to fully mask a trench filled with epitaxial silicon as instantly claimed, and in combination with the additional method steps.

Response to Arguments

10. Applicant's arguments filed July 21, 2005 have been fully considered but they are not persuasive. Applicant argues that Chen et al. fails to teach a heavily doped p+ layer around the trench pattern. However, the examiner disagrees. Chen et al., as stated in the rejection, does teach the formation of a doped layer (19) in figure 1C, which is a p-type layer that is formed by heavily doping boron atoms to a high density of 10^{18}-10^{20}

atoms/cm^3 [col. 4, lines 38-41]. Thus, the doped layer 19 is a heavily doped p+ layer as required. With regards to the arguments that the layer is not "around" the trench, it is noted that figure 3 of Applicant's disclosure defines the term "around" by showing a p+ layer (22) that is within substrate (10) and that touches three sides of trench (18). Chen et al. shows the same basic concept in figure 1C: a p+ layer (19) within substrate (1) that also touches three sides of the trench (15). Thus, the doped layer (19) is also "around" the trench since the layer is formed within the substrate and touches three sides of the trench, as required.

As such the rejections are considered to be proper.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

12/2/05

José R. Díaz
Examiner
Art Unit 2815